

SIMPLIFIED PROCESSING AND IMPROVED EFFICIENCY OF CRYSTALLINE SILICON ON GLASS MODULES

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ABSTRACT: Crystalline Silicon on Glass (CSG) is a thin-film photovoltaic solar conversion technology that has been developed from the outset to avoid the manufacturing pitfalls associated with most thin-film approaches. During the past year a further improvement in this technology has been accomplished by significantly decreasing the number of steps and relaxing the alignment tolerances required for contact formation. The simplified process sequence is described in detail, the performance of modules fabricated using this new scheme is presented, and the cost of manufacturing photovoltaic modules using this approach is discussed.

Keywords: Thin Film, Silicon, Manufacturing and Processing

1 INTRODUCTION

Pacific Solar Pty Ltd was formed in the Sydney suburb of Botany in 1995 for the express purpose of developing a photovoltaic solar conversion technology that would combine the best attributes of silicon wafer technology with the best attributes of thin-film technology. The vision from the outset has been to create a technology that could compete with conventional electricity distribution networks in many areas of the world, without relying on government subsidies to be cost effective. The technology developed involves the direct deposition of silicon onto glass followed by solid-phase crystallisation – a thin-film approach that has been designated as Crystalline Silicon on Glass (CSG) [1-3].

2 THE PROMISE AND PITFALLS OF THIN FILMS

Thin films have some clear advantages for low-cost photovoltaics. One is that the thickness of electrically active semiconductor material can be very small, typically less than 2 μm . Another is that the size of the individual units moving through the production process can be very large, sometimes more than 1 m^2 . When manufacturing photovoltaic panels, thin layers reduce material cost and large size reduces equipment and labour cost.

These cost drivers apply even to conventional wafer-based products, where growth in market share is currently being influenced to a significant degree by each manufacturer's ability to process wafers that are thinner and larger than their competitors. Crystalline Silicon on Glass technology can be viewed as the ultimate extension of this push towards very thin, very large wafers of silicon, into the regime where the silicon 'wafers' are so thin and so large that they can only be handled if they are supported by a sheet of glass.

Despite the obvious potential for thin-film photovoltaics, none of the thin-film technologies commercialised to date has been able to supersede conventional wafer-based technology. The reasons hinge on practical manufacturing issues rather than fundamental concepts, but their subtlety does not lessen their significance. The manufacturing pitfalls of thin-film photovoltaics fall into three broad categories, as follows.

Note that CSG technology has been developed specifically with the intent of avoiding these pitfalls.

2.1 "Inadequate uniformity"

It is remarkably difficult to design and build low-cost equipment for depositing thin-film materials over large areas with uniform electronic qualities. The task is even more difficult for compound semiconductors where a fixed stoichiometry is required. The investment in time and money that is required exceeds what the photovoltaic community can afford. CSG technology avoids this pitfall by using silicon deposition equipment developed for the flat-panel display industry. The KAI series of PECVD deposition equipment developed by Unaxis is particularly suitable for low-cost manufacturing. KAI systems currently being delivered to customers are capable of uniform deposition over 1.4 m^2 , with systems for even larger sheets under development.

2.2 "Inadequate durability"

It takes very little corrosion to damage a micron-thick layer, so only exceptionally stable materials can be used in a thin-film module. Materials that are sensitive to water are unsuitable and, in particular, experience has shown that transparent conducting oxides should be avoided. CSG technology avoids this pitfall by using only crystalline silicon for the electronic layer and aluminium metal for the conducting layer. These materials are so stable that CSG modules are able to survive damp heat and humidity-freeze thermal cycles without any encapsulation.

Thin films can suffer adhesion problems in outdoor use due to thermal mismatch between the semiconductor layer and its supporting substrate. Thermal mismatch is of particular concern when depositing a semiconductor material with a low thermal expansion coefficient onto soda-lime glass or a metal sheet, which have a relatively high thermal expansion coefficient. CSG technology avoids this pitfall by using borosilicate glass, which has a thermal expansion coefficient that is a good match to crystalline silicon, at around 4 ppm/K.

2.2 "Inadequate yield"

When working with individual silicon wafers, the occasional bad wafer can be easily detected and discarded before the module is assembled. This is not the case with large thin-film modules, where defects in the material are built-in from the outset and cannot be

physically removed. This problem becomes progressively worse as the number of steps in the process sequence increases, because each step can introduce additional defects. This problem is minimised with CSG technology by incorporating only a single semiconductor deposition step and by electrically isolating any defects that may be present. The electrical isolation is accomplished by ensuring that all of the highly conducting layers (there is only one with CSG technology) are interrupted at frequent intervals, providing only the conductance paths essential for normal cell operation. That way, shunts only affect the local area immediately surrounding them and have little impact on the cell as a whole.

Over the past year, the anticipated manufacturing yield of the CSG technology has been further enhanced by greatly simplifying the processes used to make metal contact to the silicon layers. The number of process steps has been significantly decreased and, importantly, the alignment tolerances required have been greatly relaxed.

3 SIMPLIFIED DEVICE PROCESSING

Over the past year, Pacific Solar has developed a simple, robust, low-cost process sequence for making electrical contact to the n and p layers in crystalline silicon films deposited onto glass. Multiple patents are pending for the key methods that underlie this contacting approach.

The completed contact structure is shown in Figure 1, where the vertical axis is greatly exaggerated relative to the horizontal axis for clarity.

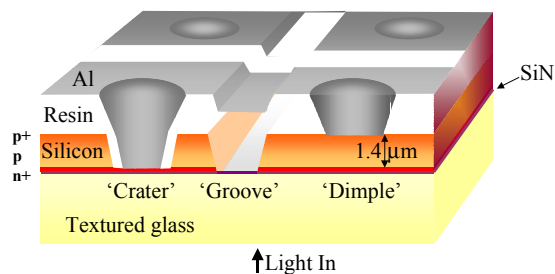


Figure 1: Schematic showing simplified contact scheme.

3.1 Silicon preparation

The preparation of the CSG layer itself is essentially unchanged from the previously published description [3]. Borosilicate float glass is textured on both surfaces by a patented dip coating process to leave a monolayer of silica beads embedded in a sol-gel matrix. An antireflection coating of silicon nitride is deposited onto one surface, followed by deposition using PECVD at 45 nm/min of 1.4 μm of amorphous silicon having an n⁺pp⁺ structure. The coated glass sheets are heated to 600°C in a batch oven process to achieve solid-phase crystallisation. Crystallographic defects are annealed by heating the silicon very briefly to over 900°C. Most of the remaining defects are passivated by exposure to atomic hydrogen.

3.2 Cell patterning

Device fabrication starts by using a pulsed laser to slice the silicon layer into a series of adjacent narrow strips, each about 6 mm wide. The module is then coated with a thin layer of novolac resin loaded with white

pigment to make it more reflective so as to improve light trapping in the silicon layer.

3.3 Crater contacts

The n-type crater contacts are formed next, and it is here that the most innovative process simplification has been implemented. An ink-jet printhead is used to dispense droplets of caustic solution wherever a crater opening is desired. Each printhead can have dozens of nozzles, and each nozzle can dispense at least a thousand droplets per second. The caustic droplets react with the resin and form water-soluble compounds that can be rinsed away, leaving the desired pattern of openings in the resin layer (patent pending). This patterning process was developed in conjunction with ink-jet specialist Xennia Technology Ltd, which has become the first licensee.

The silicon within the openings is etched in a dilute solution of HF acid and potassium permanganate that has a distinctive purple colour. After a few minutes, this 'purple etch' removes all of the p⁺ material from within the openings. In addition, a field of pinholes is formed within each opening where grain boundaries and local defects cause the silicon to be more susceptible to the etch. The n⁺ layer is exposed near the bottom of these pinholes. There is a wide range in etch time from the initial formation of sufficient pinholes for making contact until too much silicon is removed.

After etching, the p⁺ layer is removed from within the openings but is exposed along the walls of the openings. Shunting occurs when metal is deposited in the openings unless the exposed walls are protected. This is accomplished by a reflow process (patent pending), in which the resin is exposed to solvent vapour for a few minutes. This causes the resin to flow just enough to cover the sidewalls of the etched craters, but not so much as to collapse the openings completely.

3.4 Dimple contacts

A second set of openings, called dimples, is patterned using the ink-jet process. The silicon within these openings is only etched for a few seconds in purple etch to remove surface damage resulting from the hydrogen passivation process. This allows a thin layer of sputtered aluminium to make good ohmic contact to the p⁺ layer within these dimple openings, as well as making good contact to the n⁺ layer in the crater pinholes.

3.5 Metal patterning

The thin layer of aluminium is sliced into a large number of individual pads using a defocused pulsed laser. The layer of white novolac resin prevents the silicon from being heated either directly by the laser beam or indirectly from the heat of metal ablation. Each metal pad connects one line of p-type dimple contacts in one cell to a line of n-type crater contacts in the adjacent cell. Each such metal link is electrically isolated from the other metal links. This greatly reduces the impact of shunts by limiting their influence to a small local area. A micrograph of these metal links is shown in Figure 2. In this figure, the bright regions are aluminium metal and the scribe through the underlying silicon that separates the two adjacent cells runs vertically down the centre of the micrograph. The dark spots are craters and the light spots are dimples.

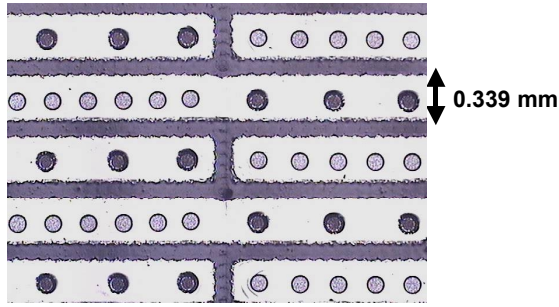


Figure 2: Metal interconnect between adjacent cells.

4 MODULE PERFORMANCE

The simplified device processing sequence has been implemented gradually over the past year in the pilot line at Pacific Solar. Modules have been produced using this sequence in two different sizes. The smaller minimodules are 96 cm² in area, composed of 20 cells in series, while the larger modules are 930 cm² in area, composed of 60 cells in series. The two different sizes have been used because specialised hydrogenation equipment suitable for processing the larger size has only recently been received from Roth&Rau AG.

Consequently, the simplified process sequence was developed first using minimodules and the processing of these smaller modules is more advanced than for larger modules. Figure 3 illustrates the current-voltage curves at four light intensities for a minimodule with an efficiency of 8.0% as measured by Sandia National Laboratories using an opaque aperture mask. This result is comparable to the best previously reported CSG module [4], which was 8.2% efficient but used a significantly more complex process to form the n-type crater contacts.

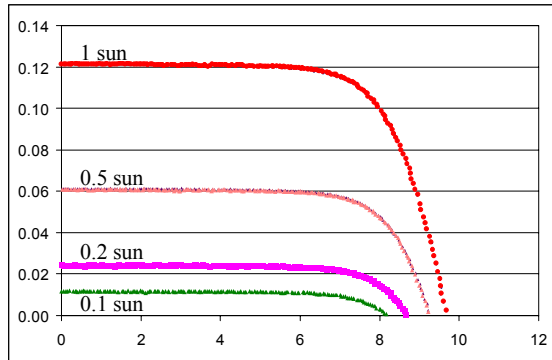


Figure 3: I-V curves for an 8% minimodule.

With future process development using the new large-area hydrogen passivation equipment, the performance of the larger modules can be expected to approach the performance obtained from the minimodules. Sampling of minimodule performance over the entire area of a 0.7-m² silicon deposition shows good performance uniformity, suggesting that the performance obtained in minimodules is representative of what might be achieved in factory production within a two-year timeframe.

5 PRODUCTION COST

The cost of manufacturing 1.4-m² CSG modules using the simplified process sequence has been calculated for a small factory located in Germany (20 MW/yr at 8%). Such a factory would have a capital cost in the absence of any subsidies of about €60 million. It would have a manufacturing floor space of 5500 m² and operate around the clock with a total workforce of 70 people.

The manufacturing cost for framed modules, packaged and ready to ship, is calculated to be €124/m². This cost includes all of the costs of operating this factory and allows for a 5% yield loss. It does not include the cost of marketing or selling the product, corporate overheads, or profit margin. This areal cost converts into a production cost (€/W), as shown in Figure 4, depending on the average aperture-area efficiency of the modules produced. The production cost is also affected by the width of inactive perimeter, assumed here to be 15 mm.

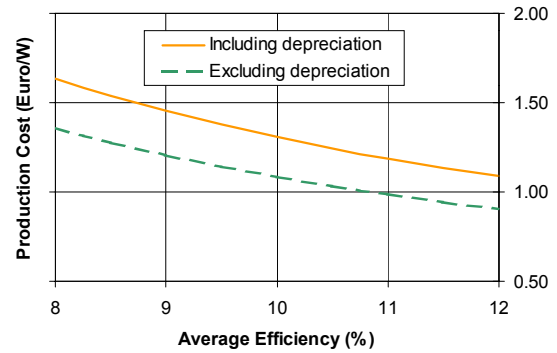


Figure 4: Production cost as a function of efficiency.

The upper curve in Figure 4 includes the cost of depreciation for equipment and infrastructure over a ten-year period, and therefore represents the ex-works sales price required for a sustainable factory operation. The lower curve excludes depreciation and therefore represents the ex-works sales price required to obtain short-term positive cash flow for the factory operation.

The production cost illustrated in Figure 4 is for the simplified process sequence that has been demonstrated to produce efficiency in the vicinity of 8% on the pilot line. Future process development work can be expected to further reduce the manufacturing cost per unit area and to increase the efficiency of the modules produced.

The production cost can be divided into four broad sectors as illustrated in Figure 5.

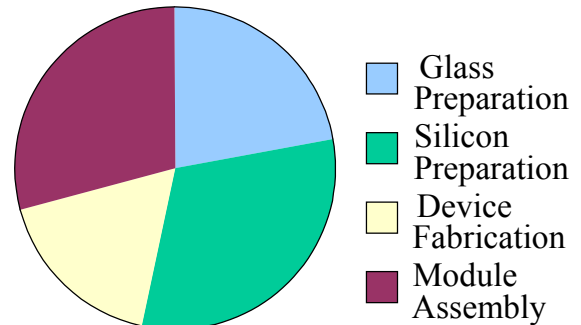


Figure 5: Production cost allocated by process sector.

The Module Assembly sector, which represents 30% of the production cost, could be performed by existing module manufacturers. This sector involves ultrasonic soldering of a plated copper tab along each edge of the module, lamination of a polymer backsheet, attachment of a junction box, aluminium framing, and packaging for shipment. Encouraging existing module manufacturers to perform these steps would make effective use of their existing sales and distribution channels and create constructive business alliances.

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